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PATENT APPLICATION

ATTORNEY DOCKET NO. 10991915-1IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Dale C. Morris, et al

Confirmation No.: 1658

Application No.: 09/499,720

Examiner: Mldys Rojas

Filing Date: February 8, 2000

Group Art Unit: 2185

Title: PRIVILEGE PROMOTION BASED ON CHECK OF PREVIOUS PRIVILEGE LEVEL

Mail Stop Appeal Brief-Patents  
Commissioner For Patents  
PO Box 1450  
Alexandria, VA 22313-1450TRANSMITTAL OF APPEAL BRIEFTransmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on June 5, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(d)) \$500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:☐ 1st Month  
\$120☐ 2nd Month  
\$450☐ 3rd Month  
\$1020☐ 4th Month  
\$1590☐ The extension fee has already been filed in this application.☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.Please charge to Deposit Account 08-2025 the sum of \$ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:  
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Signature: 

Respectfully submitted,

Dale C. Morris, et al

By: 

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Rev 10/05 (Aptent)

AUG 07 2006

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appellant: Dale C. Morris, et al.

Examiner: Midys Rojas

Serial No.: 09/499,720

Group Art Unit: 2185

Filed: February 8, 2000

Docket No.: 10991915-1

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LEVEL**APPEAL BRIEF UNDER 37 C.F.R. § 41.37****Mail Stop Appeal Brief – Patents**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed June 5, 2006, appealing the rejection of claims 1-24 of the above-identified application as set forth in the Final Office Action mailed April 5, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge **Deposit Account No. 08-2025** in the amount of **\$500.00** for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellants respectfully request consideration and reversal of the Examiner's rejection of pending claims 1-24.

08/08/2006 MBIZUNES 00000049 082025 09499720

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AUG 07 2006

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Dale C. Morris, et al Examiner: Midys Rojas  
Serial No.: 09/499,720 Group Art Unit: 2185  
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PRIVILEGE LEVEL

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**CERTIFICATE OF TELEFACSIMILE TRANSMISSION**

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Sir:

I certify that the following papers are being transmitted via telefacsimile and addressed to the U.S. Patent and Trademark Office on the date shown below:

1. Transmittal of Appeal Brief (1 pg.).
2. Appeal Brief Under 37 C.F.R. § 41.37 (25 pgs.).

Respectfully submitted,

Dale C. Morris, et al,

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**27 PAGES - INCLUDING COVER PAGE**

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**REAL PARTY IN INTEREST**

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

**RELATED APPEALS AND INTERFERENCES**

Appellants submit that there are no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal.

**STATUS OF CLAIMS**

In a Final Office Action mailed April 5, 2006, claims 1-24 were finally rejected. Claims 1-24 are pending in the application, and are the subject of the present Appeal.

**STATUS OF AMENDMENTS**

No amendments have been entered subsequent to the Final Office Action mailed April 5, 2006. The claims listed in the Claims Appendix, therefore, reflect the claims as of April 5, 2006.

**SUMMARY OF THE CLAIMED SUBJECT MATTER**

The subject matter of the independent claims involved in the Appeal is related to a method of promoting a current privilege level of a processor of a computer system controlled by an operating system, wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources.

One aspect of the present invention, as claimed in independent claim 1, provides a method (100) of promoting a current privilege level (52) of a processor (32) of a computer system (30) controlled by an operating system (36), wherein the current privilege level (52) controls application instruction (56) execution in the computer system (30) by controlling

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accessibility to system resources. The method (100) includes performing a privilege promotion instruction (62) by the operating system (36). The privilege promotion instruction (62) is stored in a first page (58) of memory (34) not writeable by application instructions (56) at a first privilege level. The privilege promotion instruction (62) includes reading a stored previous privilege level state (70) and comparing the read previous privilege level state (70) to the current privilege level (52). If the previous privilege level state (70) is equal to or less privileged than the current privilege level (52), the current privilege level (52) is promoted to a second privilege level which is higher than the first privilege level. *See Specification*, page 5, line 25 – page 10, line 19; and Figures 1 and 2.

Another aspect of the present invention, as claimed in independent claim 6, provides a method (100) of executing instructions in a computer system (30) controlled by an operating system (36). The method (100) includes executing application instructions (56) in a processor (32) of the computer system (30) at a current privilege level (52) of the processor (32) equal to a first privilege level. The application instructions (56) are stored in a first page (54) of memory (34). The current privilege level (52) controls application instruction (56) execution in the computer system (30) by controlling accessibility to system resources. The method (100) includes performing a call instruction (104) to a second page (58) of memory (34) not writeable by the application instructions (56) at the first privilege level. The call instruction (104) includes storing a return address (106) to the first page (54) of memory (34), storing the first privilege level in a previous privilege level state (70), and performing a privilege promotion instruction (62) by the operating system (36). The privilege promotion instruction (62) is stored in the second page (58) of memory (34). The privilege promotion instruction (62) includes reading the stored previous privilege level state (70) and comparing the read previous privilege level state (70) to the current privilege level (52). If the previous privilege level state (70) is equal to or less privileged than the current privilege level (52), the current privilege level (52) is promoted to a second privilege level which is higher than the first privilege level. *See Specification*, page 5, line 25 – page 10, line 19; and Figures 1 and 2.

Yet another aspect of the present invention, as claimed in independent claim 12, provides a computer system (30). The computer system (30) includes a processor (32)

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having a current privilege level (52) which controls application instruction (56) execution in the computer system (30) by controlling accessibility to system resources and having a previous privilege level state (70). The computer system (30) includes a memory (34) having a plurality of memory pages (54, 58) including a first memory page (58) storing a privilege promotion instruction (62). The first memory page (58) is not writeable by application instructions (56) at a first privilege level. The computer system (30) includes an operating system (36) stored in the memory (34) for controlling the processor (32) and memory (34) and for performing the privilege promotion instruction (62). The privilege promotion instruction (62) reads the previous privilege level state (70) and compares the read previous privilege level state (70) to the current privilege level (52). If the previous privilege level state (70) is equal to or less privileged than the current privilege level (52), the current privilege level (52) is promoted to a second privilege level which is higher than the first privilege level. *See Specification*, page 5, line 25 – page 10, line 19; and Figures 1 and 2.

Yet another aspect of the present invention, as claimed in independent claim 17, provides a computer system (30). The computer system (30) includes a processor (32) having a current privilege level (52) which controls application instruction (56) execution in the computer system (30) by controlling accessibility to system resources. The computer system (30) includes a memory (34) having a plurality of memory pages (54, 58) including a first memory page (54) storing application instructions (56) and a second memory page (58) storing a higher privileged routine (60) and a privilege promotion instruction (62). The second memory page (58) is not writeable by the application instructions (56) at a first privilege level. The computer system (30) includes an operating system (36) stored in the memory (34) for controlling the processor (32) and memory (34). The processor (32) executes the application instructions (56) with the current privilege level (52) equal to the first privilege level and the application instructions (56) perform a call instruction (104) to the second memory page (58). The call instruction (104) stores a return address (106) to the first memory page (54) and stores the first privilege level in a previous privilege level state (70). The operating system (36) performs the privilege promotion instruction (62). The privilege promotion instruction (62) reads the stored previous privilege level state (70) and compares the read previous privilege level state (70) to the current privilege level (52). If the previous

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privilege level state (70) is equal to or less privileged than the current privilege level (52), the current privilege level (52) is promoted to a second privilege level which is higher than the first privilege level. *See Specification*, page 5, line 25 – page 10, line 19; and Figures 1 and 2.

Yet another aspect of the present invention, as claimed in independent claim 23, provides a computer readable medium containing a privilege promotion instruction (62) for controlling a computer system (30) to perform a method (100) of promoting a current privilege level (52) of a processor (32) of the computer system (30). The current privilege level (52) controls application instruction (56) execution in the computer system (30) by controlling accessibility to system resources. The method (100) includes reading a stored previous privilege level state (70) and comparing the read previous privilege level state (70) to the current privilege level (52). If the previous privilege level state (70) is equal to or less privileged than the current privilege level (52), the current privilege level (52) is promoted to a privilege level which is higher than the current privilege level. *See Specification*, page 5, line 25 – page 10, line 19; and Figures 1 and 2.

**GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

- I. Whether claims 1-5, 12-16, 23, and 24 are patentable under 35 U.S.C. § 103(a) over the Arora U.S. Patent No. 6,393,556 in view of the Mattison U.S. Patent Application Publication No. 2002/0069316.
- II. Whether claims 6-11 and 17-22 are patentable under 35 U.S.C. § 103(a) over the Arora U.S. Patent No. 6,393,556 in view of the Mattison U.S. Patent Application Publication No. 2002/0069316.

**ARGUMENT**

**I. The Applicable Law**

With regard to a 35 U.S.C. § 103 obviousness rejection: "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. 2141 (emphasis in the original). The Examiner bears the burden under 35 U.S.C. § 103 in establishing a *prima*

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*facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *In re Fine* at 1074. Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375, 379 (Fed. Cir. 1986). Third, the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A. 1974).

The court in *Fine* stated:

Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

*In re Fine*, 5 USPQ2d at 1599 (citations omitted).

There must be some teaching somewhere that provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem that it addresses. *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988); *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (C.C.P.A. 1979). In particular, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon applicant's disclosure. *In re Vaack*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142 (emphasis added).

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). Furthermore, claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), *cert.*

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*denied*, 481 U.S. 1052 (1987). At the same time, a prior patent cited as a § 103 reference must be considered in its entirety, “i.e. as a *whole*, including portions that lead away from the invention.” *Id.* That is, the Examiner must recognize and consider not only the similarities, but also the critical differences between the claimed invention and the prior art as one of the factual inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (emphasis added). Finally, the Examiner must avoid hindsight. *Id.*

With regard for the test for obviousness under § 103, a statement that modifications of the prior art to meet the claimed invention would have been “ ‘well within the ordinary skill of the art’ at the time the claimed invention was made” because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); M.P.E.P. § 2143.01 (emphasis in the original).

In conclusion, an applicant is entitled to a patent grant if any one of the elements of a *prima facie* case of obviousness is not established. The Federal Circuit has endorsed this view in stating: “If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent.” *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1448 (Fed. Cir. 1992).

**II. Rejection of claims 1-5, 12-16, 23, and 24 under 35 U.S.C. § 103(a) as being unpatentable over the Arora U.S. Patent No. 6,393,556 in view of the Mattison U.S. Patent Application Publication No. 2002/0069316.**

The combination of the Arora Patent and the Mattison Publication fail to render claims 1-5, 12-16, 23, and 24 *prima facie* obvious. Appellants submit that the Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the invention of independent claims 1, 12, and 23.

The Arora Patent discloses changing a privilege level in a processor configured to pipeline instructions. The processor includes a first memory storing an architectural privilege level that is set at a first privilege level, a second memory storing a plurality of instructions,

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and a pipeline including a plurality of processing stages. A first instruction is fetched from the memory and a determination is made whether the first instruction requires the first privilege level be changed to a second privilege level, and in response thereto, any subsequent instructions are flushed from the pipeline before recording the second privilege level in the first memory. (Abstract).

In the Arora Patent, the processor 30 maintains a "current privilege level" (CPL) 38 in a memory storage device. The CPL is maintained in the processor's register set. The operating system sets the CPL to prevent the user from performing dangerous or insecure operations. If the pipeline 30 is currently processing an application program instruction, a prior instruction would have set the CPL 38 to the proper privilege level. If an instruction requiring a higher privilege level follows the current instruction, an instruction, such as an "enter privilege code" (EPC) instruction, that directs the processor to change the privilege level of the CPL must first be processed to increase the privilege level. (Col. 4, lines 13-27).

In the Arora Patent, after decoding an instruction directing the processor to change the CPL 38 from a first to a second privilege level, the processor compares the second privilege level to the CPL 38. (Col. 6, lines 27-31). The processor will compare the CPL 38 with the privilege level specified in the EPC instruction. If the EPC instruction directs the processor to change the CPL 38 to a higher privilege level, the processor flushes any instructions in the pipeline subsequent to the EPC instruction, and continues processing the EPC instruction. When the EPC instruction is retired, the CPL 38 privilege level is increased. If the EPC instruction specifies a privilege level lower than or the same as the CPL 38, the processor will issue a fault. (Col. 6, lines 46-59).

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current

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**privilege level to a second privilege level which is higher than the first privilege level as recited in independent method claim 1.**

The Examiner admits that the Arora Patent does not disclose storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. (Final Office Action mailed April 5, 2006, page 5). The Examiner submits that the Mattison Publication discloses this claim limitation in paragraphs 0015 and 0016.

The Mattison Publication discloses a method and apparatus for protecting flash memory such as a Basic Input/Output System (BIOS) from any unauthorized reprogramming efforts. The system includes a memory controller that provides a mode where the processor is restricted to accessing only the flash memory (i.e., a mode where the processor can only execute instructions from the flash memory and not from any other memory such as main system memory or cache). This mode can be enabled or disabled by setting or clearing a control register of the system memory controller. In addition, the memory controller incorporates a set of registers that can be used to define limited regions of accessibility to memory space outside flash memory. These registers are accessible to the processor only when the controller is operating in the restricted access mode. The register set consists of one or more pairs of registers, wherein each pair consists of a base register and a limit register. The base and limit registers define a memory region beyond the flash memory which would be accessible to the processor when the system is operating in the restricted mode. (Paragraphs 0015-0016).

The flash memory protection disclosed by the Mattison Publication does not teach or suggest the privilege promotion instruction being stored in a first page of memory not writable by application instructions at a first privilege level as recited in claim 1. The flash memory protection system disclosed by the Mattison Publication is not related to privilege levels. In contrast, the flash memory protection system is just a mode of operation initiated by a flash memory upgrade program. (Paragraph 0019). The Mattison Publication fails to teach or suggest privilege levels or a first page of memory not writable by application instructions at a first privilege level.

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The Examiner states that the claim 1 limitations of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level is disclosed in column 6, lines 46-49 of the Arora Patent. (Final Office Action mailed April 5, 2006, page 4). The Examiner also states that the previous privilege level state is disclosed by CPL 38 of the Arora Patent. (Final Office Action mailed April 5, 2006, page 4). In addition, the Examiner states that "comparing the current privilege level to the instruction's privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level." (Final Office Action mailed April 5, 2006, page 4).

The cited text of the Arora Patent discloses comparing the architectural CPL with the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent fails to disclose the claim 1 limitations of *reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level*. In the Arora Patent, a previous privilege level state is not stored and therefore cannot be read.

The Arora Patent also discloses that the CPL is compared to the privilege level specified in the EPC instruction. In contrast, claim 1 requires comparing the *read previous privilege level state to the current privilege level*. The privilege level of the EPC instruction does not teach or suggest the current privilege level. Rather, the EPC instruction directs the processor to change the privilege level of the CPL. (Col. 4, lines 24-26). The EPC instruction provides a potential future privilege level, not the current privilege level. The Arora Patent discloses that an EPC instruction *eventually may* cause the processor 30 to change the architectural CPL 38 to a second privilege level. (Col. 4, lines 56-58).

The Examiner states that the claim 1 limitations of "if a previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level" are disclosed by the Arora Patent "since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level . . .". (" . . . increase the architectural current privilege level from privilege level 3 to privilege level 0"). (Final Office Action mailed April 5, 2006, page 5). The Examiner further states that, in comparing privilege levels, it is

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understood that the stored privilege level (stored in CPL 38) must be read in the comparison process. (Final Office Action mailed April 5, 2006, page 5).

The Arora Patent discloses raising the current architectural CPL to the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent, however, does not disclose the claim 1 limitation of promoting the current privilege level to a second privilege level which is higher than the first privilege level if the previous privilege level state is equal to or less privileged than the current privilege level.

Claim 1 recites if the *previous privilege level state is equal to or less privileged than the current privilege level*, promoting the current privilege level. In contrast, the Examiner states that the Arora Patent discloses increasing the *current privilege level* if the privilege level of the CPL is *lower* than the privilege level of the EPC. The Arora Patent discloses if the EPC instruction specifies a privilege level lower than, *or the same as*, the architectural CPL, the processor will issue a fault rather than promote the CPL. (Col. 6, lines 56-59). In addition, the Examiner states that the privilege level of the EPC instruction discloses the current privilege level state and the CPL discloses the stored previous privilege level state. (Final Office Action mailed April 5, 2006, pages 4-5). Further, the Examiner states that the privilege level of the EPC instruction is the privilege level necessary for the instruction that is currently being prepared for execution in the system, thus it is a current privilege level; and that the CPL is the previous privilege level because it was the privilege level necessary for the execution of a previous instruction. (Final Office Action mailed April 5, 2006, pages 2-3). Therefore, based on the Examiner's interpretation, claim 1 would recite if the CPL is equal to or less privileged than the privilege level of the EPC instruction, promoting the current privilege level. The CPL, however, is the current privilege level, not the previous privilege level state, and the privilege level of the EPC instruction is a future privilege level, not the current privilege level as submitted by the Examiner. The CPL in the Arora Patent is not increased to the privilege level of the EPC instruction until the EPC instruction is retired. (Col. 6, lines 54-56).

Further, there is no teaching or suggestion to combine the Arora Patent with the Mattison Publication in a manner that would provide the invention of independent claim 1. The Arora Patent is directed to an apparatus and method for changing a privilege level in a

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processor configured to pipeline instructions. In contrast, the Mattison Publication is directed to a method and apparatus for protecting flash memory and is not related to pipeline instructions or privilege levels. The Arora Patent and the Mattison Publication address unrelated problems. One skilled in the art would not look to the Mattison Publication when designing an apparatus and method for changing privilege levels. One skilled in the art could not combine the apparatus and method for changing the privilege level in a processor configured to pipeline instructions of the Arora Patent with the flash memory protection system of the Mattison Publication in a manner that would provide the invention recited by independent claim 1.

In view of the above, Appellants believe independent claim 1 to be allowable over the Arora Patent and the Mattison Publication. Dependent claims 2-5 further define patentably distinct independent claim 1. Accordingly, dependent claims 2-5 are also believed to be allowable over the Arora Patent and the Mattison Publication.

The Arora Patent and the Mattison Publication, either alone, or in combination, also fail to teach or suggest the computer system of independent claim 12 including a **memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the first memory page is not writeable by application instructions at a first privilege level; and performing the privilege promotion instruction as follows: reads the previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

The Arora Patent and the Mattison Publication, either alone, or in combination, also fail to teach or suggest the computer readable medium of independent claim 23 containing a privilege promotion instruction for controlling a computer system to perform a method including **reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.**

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For the same reasons as discussed above with reference to independent claim 1, the Arora Patent and the Mattison Publication fail to teach or suggest the above limitations of independent claims 12 and 23, which are similar to the above limitations of independent claim 1.

In view of the above, Appellants believe independent claims 12 and 23 to be allowable over the Arora Patent and the Mattison Publication. Dependent claims 13-16 further define patentably distinct independent claim 12, and dependent claim 24 further defines patentably distinct independent claim 23. Accordingly, dependent claims 13-16 and 24 are also believed to be allowable over the Arora Patent and the Mattison Publication.

In view of the above, Appellants respectfully request reversal of the rejection of claims 1-5, 12-16, 23, and 24 under 35 U.S.C. § 103(a).

**III. Rejection of claims 6-11 and 17-22 under 35 U.S.C. § 103(a) as being unpatentable over the Arora U.S. Patent No. 6,393,556 in view of the Mattison U.S. Patent Application Publication No. 2002/0069316.**

The combination of the Arora Patent and the Mattison Publication fail to render claims 6-11 and 17-22 *prima facie* obvious. Appellants submit that the Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the invention of independent claims 6 and 17.

The Arora Patent and the Mattison Publication were described above in Section II of the Argument.

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including: storing the first privilege level in a previous privilege level state; and performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including: reading the stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level,

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**promoting the current privilege level to a second privilege level which is higher than the first privilege level as recited in independent method claim 6.**

For the same reasons as discussed above with reference to independent claim 1 in Section II of the Argument, the Arora Patent and the Mattison Publication fail to teach or suggest the above limitations of claim 6, which are similar to the above limitations of claim 1.

In addition, the Arora Patent and the Mattison Publication fail to teach or suggest *storing the first privilege level in a previous privilege level state*. The Examiner submits that the CPL 38 is the previous privilege level state and the privilege level of the EPC instruction is the current privilege level. (Final Office Action mailed April 5, 2006, pages 4-5). The Examiner also submits that the privilege level of the EPC instruction is the privilege level necessary for the instruction that is currently being prepared for execution in the system, thus it is a current privilege level; and that the CPL is the previous privilege level because it was the privilege level necessary for the execution of a previous instruction. (Final Office Action mailed April 5, 2006, pages 2-3).

Claim 6, however, recites *executing application instructions in a processor of the computer system at a current privilege level of the processor equal to a first privilege level, and wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources*. The current privilege level as recited in claim 6 is not the privilege level of previous instructions but rather the privilege level for currently executing instructions. Further, in the Arora Patent the CPL is never stored in a previous privilege level state. The CPL is increased when an EPC instruction is retired. (Col. 6, lines 54-56). The Arora Patent discloses a current privilege level and a privilege level of an EPC instruction (which is a *future privilege level*) as opposed to the current privilege level and the stored *previous privilege level state* as recited by claim 6.

In view of the above, Appellants believe independent claim 6 to be allowable over the Arora Patent and the Mattison Publication. Dependent claims 7-11 further define patentably distinct independent claim 6. Accordingly, dependent claims 7-11 are also believed to be allowable over the Arora Patent and the Mattison Publication.

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the computer system of independent claim 17 including a **memory having a**

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plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privileged routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level; wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows: stores the first privilege level in a previous privilege level state; and wherein the operating system performs the privilege promotion instruction as follows: reads the stored previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.

For the same reasons as discussed above with reference to independent claim 6, the Arora Patent and the Mattison Publication fail to teach or suggest the above limitations of independent claim 17, which are similar to the above limitations of independent claim 6.

In view of the above, Appellants believe independent claim 17 to be allowable over the Arora Patent and the Mattison Publication. Dependent claims 18-22 further define patentably distinct independent claim 17. Accordingly, dependent claims 18-22 are also believed to be allowable over the Arora Patent and the Mattison Publication.

In view of the above, Appellants respectfully request reversal of the rejection of claims 6-11 and 17-22 under 35 U.S.C. § 103(a).

### **CONCLUSION**

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious the pending claims of the Present Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-24 be allowed.

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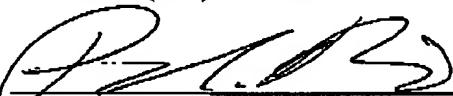
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**CERTIFICATE UNDER 37 C.F.R. 1.8:** The undersigned hereby certifies that this paper or papers, as described herein, are being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300 on this 7th day of August, 2006.

By   
Name: Patrick G. Billig

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**CLAIMS APPENDIX**

1. (Original) A method of promoting a current privilege level of a processor of a computer system controlled by an operating system, wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources, the method comprising:

performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including:

reading a stored previous privilege level state;

comparing the read previous privilege level state to the current privilege level; and

if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.

2. (Original) The method of claim 1 wherein the step of performing the privilege promotion instruction further includes:

if the previous privilege level state is more privileged than the current privilege level, taking an illegal operation fault.

3. (Original) The method of claim 1 wherein the system resources include system registers.

4. (Original) The method of claim 1 wherein the system resources include system instructions.

5. (Original) The method of claim 1 wherein the system resources include memory pages.

6. (Original) A method of executing instructions in a computer system controlled by an operating system, the method comprising:

executing application instructions in a processor of the computer system at a current privilege level of the processor equal to a first privilege level, wherein the application

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instructions are stored in a first page of memory, and wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources;

performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including:

storing a return address to the first page of memory; and

storing the first privilege level in a previous privilege level state; and

performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including:

reading the stored previous privilege level state;

comparing the read previous privilege level state to the current privilege level;

and

if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level.

7. (Original) The method of claim 6 further comprising:

performing a return instruction including:

transferring instruction control flow to the stored return address to the first page of memory; and

demoting the current privilege level to the stored previous privilege level state.

8. (Original) The method of claim 6 wherein the step of performing the privilege promotion instruction further includes:

if the previous privilege level state is more privileged than the current privilege level, taking an illegal operation fault.

9. (Original) The method of claim 6 wherein the system resources include system registers.

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10. (Original) The method of claim 6 wherein the system resources include system instructions.

11. (Original) The method of claim 6 wherein the system resources include memory pages.

12. (Original) A computer system comprising:

a processor having a current privilege level which controls application instruction execution in the computer system by controlling accessibility to system resources and having a previous privilege level state;

a memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the first memory page is not writeable by application instructions at a first privilege level; and

an operating system stored in the memory for controlling the processor and memory, and performing the privilege promotion instruction as follows:

reads the previous privilege level state;

compares the read previous privilege level state to the current privilege level;

and

if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.

13. (Original) The computer system of claim 12 wherein the operating system performing the privilege promotion instruction further includes:

if the previous privilege level state is more privileged than the current privilege level, taking an illegal operation fault.

14. (Original) The computer system of claim 12 further comprising:

system registers, and wherein the system resources include the system registers.

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15. (Original) The computer system of claim 12 wherein the system resources include system instructions.

16. (Original) The computer system of claim 12 wherein the system resources include memory pages.

17. (Original) A computer system comprising:

a processor having a current privilege level which controls application instruction execution in the computer system by controlling accessibility to system resources;

a memory having a plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privileged routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level;

an operating system stored in the memory for controlling the processor and memory;  
wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows:

stores a return address to the first memory page; and

stores the first privilege level in a previous privilege level state; and

wherein the operating system performs the privilege promotion instruction as follows:

reads the stored previous privilege level state;

compares the read previous privilege level state to the current privilege level;

and

if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.

18. (Original) The computer system of claim 17 wherein the processor via the higher privileged routine performs a return instruction as follows:

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transfers instruction control flow to the stored return address to the first page of memory; and

demotes the current privilege level to the stored previous privilege level state.

19. (Original) The computer system of claim 17 wherein the operating system performing the privilege promotion instruction further includes:

if the previous privilege level state is more privileged than the current privilege level, taking an illegal operation fault.

20. (Original) The computer system of claim 17 further comprising:

system registers, and wherein the system resources include the system registers.

21. (Original) The computer system of claim 17 wherein the system resources include system instructions.

22. (Original) The computer system of claim 17 wherein the system resources include memory pages.

23. (Original) A computer readable medium containing a privilege promotion instruction for controlling a computer system to perform a method of promoting a current privilege level of a processor of the computer system, wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources, the method comprising:

reading a stored previous privilege level state;

comparing the read previous privilege level state to the current privilege level; and

if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.

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24. (Original) The computer readable medium of claim 23 wherein the method of promoting the current privilege level further comprises:

if the previous privilege level state is more privileged than the current privilege level, taking an illegal operation fault.

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**EVIDENCE APPENDIX**

None.

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**RELATED PROCEEDINGS APPENDIX**

None.